AMENDMENTS TO THE CLAIMS

1. (original) [[A refresh circuit that controls a refresh operation of a memory array, said refresh circuit]] A memory refresh circuit comprising:

   a control circuit for conducting a memory refresh operation and for indicating when said refresh operation is complete.

2. (original) The circuit of claim 1, wherein said refresh circuit includes a refresh counter.

3. (original) The circuit of claim 1, wherein said refresh circuit comprises a refresh complete circuit for indicating when said refresh operation is complete.

4. (original) The circuit of claim 3, wherein said refresh complete circuit provides a signal indicating when said refresh operation is complete.

5. (current amended) A memory device, comprising:

   a memory array; and

   a refresh circuit [[that controls]] for controlling a refresh operation of the memory array [[, said refresh circuit]] and for indicating when said refresh operation is complete.

6. (original) The memory device of claim 5, wherein said refresh circuit includes a refresh counter.

7. (original) The memory device of claim 5, wherein said refresh circuit comprises a refresh complete circuit for indicating when said refresh operation is complete.

8. (original) The memory device of claim 7, wherein said refresh complete circuit provides a signal indicating when said refresh operation is complete.

9. (original) The memory device of claim 5, further comprising a control logic circuit that controls an operation of said memory array, said control logic circuit providing a first control signal to said refresh circuit, said refresh circuit providing a second control signal to said control logic circuit.

10. (original) The memory device of claim 9, further comprising an address multiplexer for providing a memory address to said memory array, said address multiplexer receiving control signals from said control logic circuit.

11. (original) The memory device of claim 10, wherein said address multiplexer is operational in a first mode and a second mode, said address multiplexer providing the memory address from an external source in said first mode, said address multiplexer providing the memory address from said refresh circuit in said second mode.

12. (currently amended) A memory system, comprising:

a set of memory devices, each comprising:

a memory array;

a refresh circuit coupled to said memory array for controlling a refresh operation of said memory array [[, said refresh circuit]] and for providing a refresh complete signal indicating when said refresh operation is complete; and

a combining circuit [[that combines]] for combining the refresh complete signals from the memory devices to obtain a combined refresh complete signal.

13. (original) The memory system of claim 12, wherein said refresh circuit includes a refresh counter.

14. (original) The memory system of claim 12, wherein said combining circuit includes a wired-or circuit.

15. (original) The memory system of claim 12, further comprising a power management circuit coupled to said memory devices for controlling power provided to said memory devices.

16. (currently amended) The memory system of claim 15, wherein said power management circuit is adapted to receive [[receives]] the combined refresh complete signal.

17. (original) The memory system of claim 15, wherein said power management circuit controller further comprises a micro-controller for controlling an operation of said power management controller.

18. (original) The memory system of claim 17, wherein said power management controller is coupled to a power management bus network.

19. (original) The memory system of claim 17, wherein said power management controller further comprises a temperature integration circuit for incorporating temperature into a refresh operation.

20. (original) The memory system of claim 19, wherein said temperature integration circuit is adapted to receive signals from a temperature sensor for measuring temperature.

21. (original) The memory system of claim 20, wherein said temperature sensor is located outside said memory system.

22. (original) The memory system of claim 20, wherein said temperature sensor is located inside said memory system.

23. (original) The memory system of claim 20, wherein said temperature sensor is located close to said memory array.

24. (currently amended) A memory system, comprising:

a power management circuit, comprising:

a micro-controller for controlling an operation of said power management circuit;

an input-output port circuit for inputting signals from and providing signals to other circuits;

a set of memory devices, each comprising:

a memory array;

a refresh circuit coupled to said memory array for controlling a refresh operation of said memory array[[, said refresh circuit]] and for providing a refresh complete signal indicating when said refresh operation is complete; and

a combining circuit [[that combines]] for combining the refresh complete signals from the memory devices to obtain a combined refresh complete signal, said combining circuit includes a wired-or circuit;

wherein said power management circuit adapted to receive [[receives]] the combined refresh complete signal through the input-output port and, partially in response, [[controls]] for controlling power provided to each of said memory devices, said power management circuit being coupled to each of said memory devices.

25. (original) The memory system of claim 24, wherein said power management controller is coupled to a power management bus network.

26. (original) The memory system of claim 25, wherein said power management memory circuit incorporates a read-only memory (ROM) circuit.

27. (original) The memory system of claim 25, wherein said power management memory circuit incorporates a random access memory (RAM) circuit.

28. (original) The memory system of claim 25, wherein said power management controller further comprises a temperature integration circuit for incorporating temperature into a refresh operation.

29. (original) The memory system of claim 28, wherein said temperature integration circuit is adapted to receive signals from a temperature sensor for measuring temperature.

30. (original) The memory system of claim 28, wherein said temperature sensor is located outside said memory system.

31. (original) The memory system of claim 28, wherein said temperature sensor is located inside said memory system.

32. (original) The memory system of claim 28, wherein said temperature sensor is located close to said memory array.

33. (original) The memory system of claim 25, wherein said power management controller further comprises a internetwork control circuit for coupling said power management bus network to other external circuits.

34. (original) The memory system of claim 33, wherein said internetwork control circuit is an I^2C interface.

35. (currently amended) A memory system, comprising:

a set of memory devices;

a power management circuit [[that controls]] <u>for controlling</u> power provided to each of said memory devices, said power management circuit being coupled to each of said memory devices; the power management circuit comprising:

a micro-controller for controlling an operation of said power management circuit; and

a temperature integration circuit for incorporating temperature into a refresh operation.

36. (original) The memory system of claim 35, wherein said temperature integration circuit is adapted to receive signals from a temperature sensor for measuring temperature.

37. (original) The memory system of claim 36, wherein said temperature sensor is located outside said memory system.

38. (original) The memory system of claim 36, wherein said temperature sensor is located inside said memory system.

39. (original) The memory system of claim 36, wherein said temperature sensor is located close to said memory array.

40. (original) The memory device of claim 35, wherein said refresh circuit includes a refresh counter.

41. (original) The memory device of claim 40, wherein said refresh circuit comprises a refresh complete circuit for indicating when said refresh operation is complete.

42. (currently amended) A memory system, comprising:

a memory array;

a refresh circuit [[that controls]] <u>for controlling</u> a refresh operation of the memory array[[, said refresh circuit]] <u>and for</u> indicating when said refresh operation is complete; and

a power management circuit, comprising:

a micro-controller for controlling an operation of said power management circuit;

an input-output port circuit for inputting signals from and providing signals to other circuits; and

a temperature integration circuit for incorporating temperature into a refresh operation.

43. (original) The memory device of claim 42, wherein said refresh circuit includes a refresh counter.

44. (original) The memory device of claim 43, wherein said refresh circuit comprises a refresh complete circuit for indicating when said refresh operation is complete.

45. (currently amended) A memory device comprising:

refresh circuitry [[that controls]] for controlling a refresh operation in a memory device; and

a sensor [[that senses]] for sensing an environmental condition of the memory device;

wherein said refresh circuitry is adapted to initiate [[initiating]] the refresh operation partially in response to the environmental condition sensed by the sensor, said refresh circuitry adapted to indicate when said refresh operation is complete.

46. (original) The device of claim 45, wherein said sensor is a temperature sensor.

47. (original) The device of claim 46, wherein said temperature sensor is located outside said memory system.

48. (original) The device of claim 46, wherein said temperature sensor is located inside said memory system.

49. (original)The device of claim 46, wherein said temperature sensor is located close to said memory array.

50. (original) A method of refreshing memory, comprising:

performing a burst self-refresh operation on a memory array; and

providing a refresh complete signal when said burst self-refresh operation has been completed.

51. (original) The method of claim of 50, further comprising the step of determining a pre-refresh mode of said memory array before performing said burst self-refresh operation.

52. (original) The method of claim of 51, wherein said pre-refresh mode is either a first or second mode.

53. (original) The method of claim of 52, wherein said first mode is a low-power mode.

54. (original) The method of claim 53, wherein said low-power mode is a power-off mode.

55. (original) The method of claim of 52, wherein said second mode is a higher-power mode.

56. (original) The method of claim of 52, further comprising the step of changing said memory array to said second mode before said performing said refresh operation, if said pre-refresh mode is said first mode.

57. (original) The method of claim of 50, further comprising the steps of:

measuring an ambient temperature; and

initiating said refresh operation at a certain rate if said ambient temperature is in a first set of refresh temperature values.

58. (original) The method of claim of 57, wherein said first set of refresh temperature values are pre-determined temperatures.

59. (original) The method of claim of 57, further comprising the step of integrating said ambient temperature after measuring said ambient temperature.

60. (original) The method of claim of 57, wherein said first set of refresh temperature values are pre-determined values based on integrated temperature values.

61. (original) A method of refreshing memory devices, each with a memory array the method comprising:

performing a refresh operation in a subset of the memory devices;

providing a refresh complete signal from each memory device in the subset when the memory device completes the refresh operation; and

combining the refresh signals to obtain a combined refresh complete signal.

62. (currently amended) An integrated circuit, comprising:

a memory device, comprising:

a memory array; and

a refresh circuit [[that controls]] <u>for controlling</u> a refresh operation of the memory array[[, said refresh circuit]] <u>and for</u> indicating when said refresh operation is complete.

63. (original) The integrated circuit of claim 62, wherein said refresh circuit includes a refresh counter.

64. (original) The integrated circuit of claim 62, wherein said refresh circuit comprises a refresh complete circuit for indicating when said refresh operation is complete.

65. (currently amended) The integrated circuit of claim 64, wherein said refresh complete circuit for providing [[provides]] a signal indicating when said refresh operation is complete.

66. (currently amended) The integrated circuit of claim 62, further comprising a control logic circuit for controlling [[that controls]] an operation of said memory array, said control logic circuit adapted to provide [[providing]] a first control signal to said refresh circuit, said refresh circuit provide [[providing]] a second control signal to said control logic circuit.

67. (currently amended) The integrated circuit of claim 66, further comprising an address multiplexer for providing a memory address to said memory array, said address multiplexer adapted to receive [[receiving]] control signals from said control logic circuit.

68. (currently amended) The integrated circuit of claim 67, wherein said address multiplexer is operational in a first mode and a second mode, said address multiplexer adapted to provide [[providing]] the memory address from an external source in said first mode, said address multiplexer adapted to provide [[providing]] the memory address from said refresh circuit in said second mode.

69. (currently amended) An integrated circuit, comprising:

a memory device comprising:

refresh circuitry [[that controls]] for controlling a refresh operation in a memory device; and

a sensor [[that senses]] for sensing an environmental condition of the memory device;

wherein said refresh circuitry adapted to initiate [[initiating]] the refresh operation partially in response to the environmental condition sensed by the sensor, said refresh circuitry adapted to indicate when said refresh operation is complete.

70. (original) The integrated circuit of claim 69, wherein said sensor is a temperature sensor.

71. (original) The integrated circuit of claim 70, wherein said temperature sensor is located outside said memory system.

72. (original) The integrated circuit of claim 70, wherein said temperature sensor is located inside said memory system.

73. (original) The integrated circuit of claim 70, wherein said temperature sensor is located close to said memory array.

74. (currently amended) A processor system, comprising:

a processor, and

a memory device, comprising:

a memory array; and

a refresh circuit [[that controls]] for controlling a refresh operation of the memory array[[, said refresh circuit]] and for indicating when said refresh operation is complete.

75. (original) The processor system of claim 74, wherein said refresh circuit includes a refresh counter.

76. (original) The processor system of claim 74, wherein said refresh circuit provides a refresh complete circuit for indicating when said refresh operation is complete.

77. (original) The processor system of claim 76, wherein said refresh complete circuit provides a signal indicating when said refresh operation is complete.

78. (currently amended) The processor system of claim 74, further comprising a control logic circuit [[that controls]] for controlling an operation of said memory array [[, said control logic circuit]] and for providing a first control signal to said refresh circuit [[, said refresh circuit providing and a second control signal to said control logic circuit.

79. (currently amended) The processor system of claim 78, further comprising an address multiplexer for providing a memory address to said memory array, said address multiplexer adapted to receive [[receiving]] control signals from said control logic circuit.

80. (currently amended) The processor system of claim 79, wherein said address multiplexer is operational in a first mode and a second mode, said address multiplexer adapted to provide [[providing]] the memory address from an external source in said first mode[[, said address multiplexer providing]] and the memory address from said refresh circuit in said second mode.

81. (currently amended) A processor system, comprising:

a processor, and

a memory device comprising:

refresh circuitry [[that controls]] for controlling a refresh operation in a memory device; and

a sensor [[that senses]] for sensing an environmental condition of the memory device;

wherein said refresh circuitry adapted to initiate [[initiating]] the refresh operation partially in response to the environmental condition sensed by the sensor, said refresh circuitry adapted to indicate when said refresh operation is complete.

82. (original) The processor system of claim 81, wherein said sensor is a temperature sensor.

83. (original) The processor system of claim 82, wherein said temperature sensor is located outside said memory system.

84. (original) The processor system of claim 82, wherein said temperature sensor is located inside said memory system.

85. (original) The processor system of claim 82, wherein said temperature sensor is located close to said memory array.